

# Visual Computing Colloquium

## December 11th, 2018

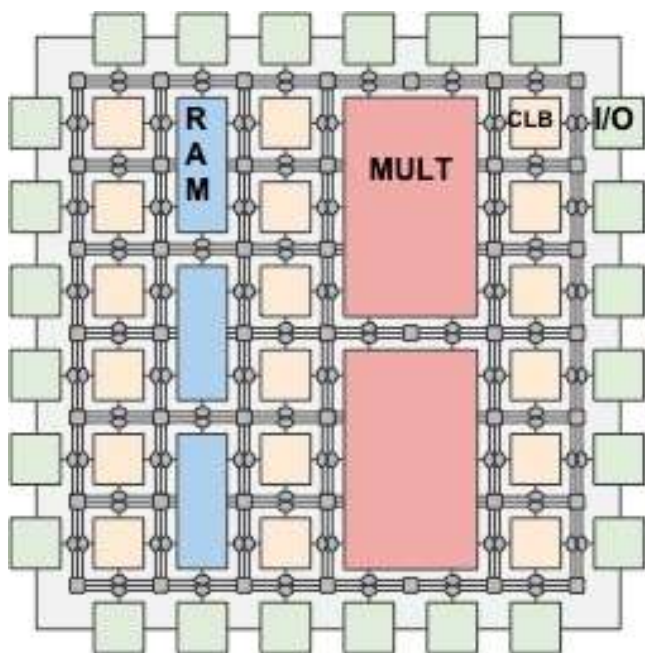
### Enhancing Academic Tools for Exploring Next Generation Mobile

**Prof. Dr. Ken Kent**

IBM Centre for Advanced Studies - Atlantic  
University of New Brunswick  
Honorary Professor at the Dept. of Computer  
Science, H-BRS

**Tuesday, Dec 11th, 2018, 5 pm**  
**Laboratory C 061**

Hochschule Bonn-Rhein-Sieg  
University of Applied Sciences  
**Institut of Visual Computing**  
Grantham-Allee 20  
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#### **Abstract:**

VTR (verilog-to-routing) is an open-source computer-aided design (CAD) flow for Field Programmable Gate Arrays (FPGA) developed in collaboration between the University of New Brunswick and the University of Toronto. The power of the tool suite is that it can target a virtual FPGA device. Unlike vendor specific tools, VTR can be used to evaluate prototype architectures of new configurable logic devices. Companies such as Google and Huawei have recently expressed interest in VTR as a solution to their internal efforts to explore configurable logic for higher performance. In particular, there is considerable interest in exploring custom architectures that can provide dedicated logic and processors for applications in the machine learning domain. In this talk, I will present an overview of the VTR tool suite and some of the projects that we are working on at the University of New Brunswick to move the software from academia to industry.

#### **Vita:**

Dr. Kenneth Kent received his Ph.D. degree in computer science from the University of Victoria in 2003. He has worked for the University of New Brunswick since 2002 in The Faculty of Computer Science where in 2009 he formed the Centre for Advanced Studies - Atlantic. He is an Honorary Professor at Hochschule Bonn-Rhein-Sieg since 2013. Dr. Kent has expertise in Field Programmable Gate Arrays (FPGA), Computer-Aided Design (CAD), virtual machines, embedded systems and high performance computing. His work in FPGA/CAD has led to the release of verilog-to-routing (VTR), an open-source software tool for packing, placing and routing verilog circuits on an FPGA. He has co authored many journal/conference papers and has 7 patents pending. He is a steering committee member of IEEE International Symposium on Rapid Systems Prototyping and International Conference on Computer Science and Software Engineering (CASCON). He has served as general and program chairs at numerous academic conferences such as IEEE RSP and IEEE HEART. Dr. Kent has also served as chair of the NSERC Strategic Grants selection committee and committee member of several national and international grant committees.

