FPGA-based Image Combining for Parallel Rendering

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electronic displays, March 2010, Nürnberg, Germany

Outline:

- Application Areas
- Parallel Rendering
- State-of-the-Art
- PixelStrom Approach
- Implementation
- Summary

Application Areas for Rendering

- Rendering of large models is used in Virtual Reality (VR) applications like:
  - Engineering, e.g. crash tests (top)
  - Design and architecture (bottom)
  - Flight and naval simulators
  - Medicine, e.g. visualization of minimal invasive operation
  - Entertainment

(Image: wwww.anl.gov)

Need for high computing power

- Complex models with many details
- Real-time for interactive manipulation
  - Different viewing angles
  - Walk through building
  - Interaction with scene

➔ Parallel rendering

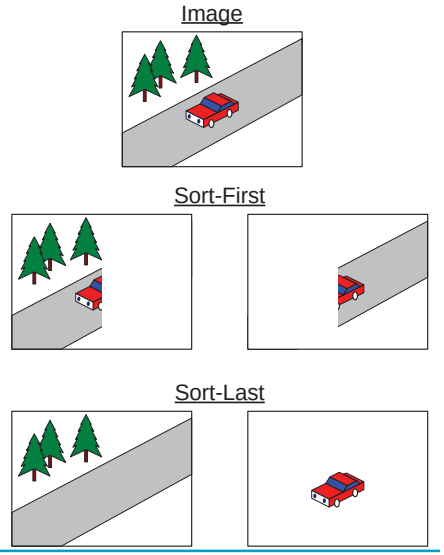
(Image: wwww.imsys-vr.com)

Parallel Rendering of Complex Scenes

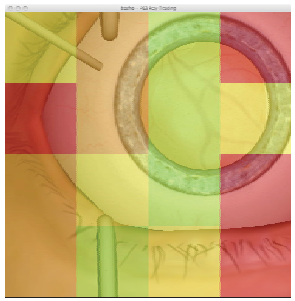
Two strategies for parallel rendering

- Sort-first
  - **Image** is divided into several regions
- Sort-last
  - **Objects** are divided between processors
  - Depth-information determines visible object

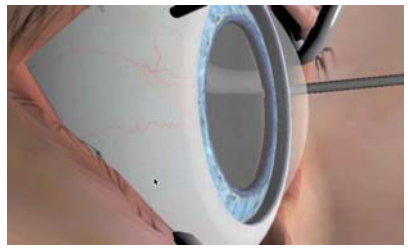
➔ Both strategies are used



Example: Parallel Rendering



Subdivision of view port into tiles



Composited image

- Project TraCell: Rendering Cluster for interactive ray tracing
- Eye rendered in parallel on cell processor of PS3 consoles
  - Sort-First strategy with variable subdivision
  - Colors on subdivision image indicate rendering node

Available Systems for Parallel Rendering

- Data exchange between two (or up to four) graphic cards
  - Nvidia Scalable Link Interface (SLI)
  - ATI Crossfire
  - ➔ CPU power limits speed-up
- Parallel computers with data exchange on network (LAN)
  - TraCell
  - ➔ High load on network limits speed-up
- Parallel computers, merging graphic cards output with external box
  - ➔ PixelStrom

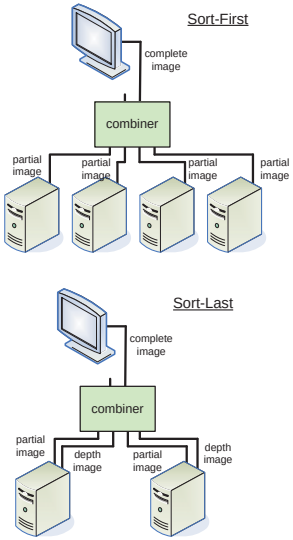
PixelStrom Approach

- Low-cost solution for merging partial results of parallel rendering
  - Parallel rendering on different PCs
  - Output on graphics port
  - FPGA-based external box for merging of graphic streams
- Approach:
  - Genlocking of graphic cards
  - Only small synchronization effort for FPGA-box
  - Supporting "sort-first" and "sort-last"
- BMBF-funded Project "PixelStrom"
  - Software
    - Parallelization of rendering, genlock
  - Hardware
    - FPGA-based combiner, synchronization of graphic signals

FPGA-based Combiner

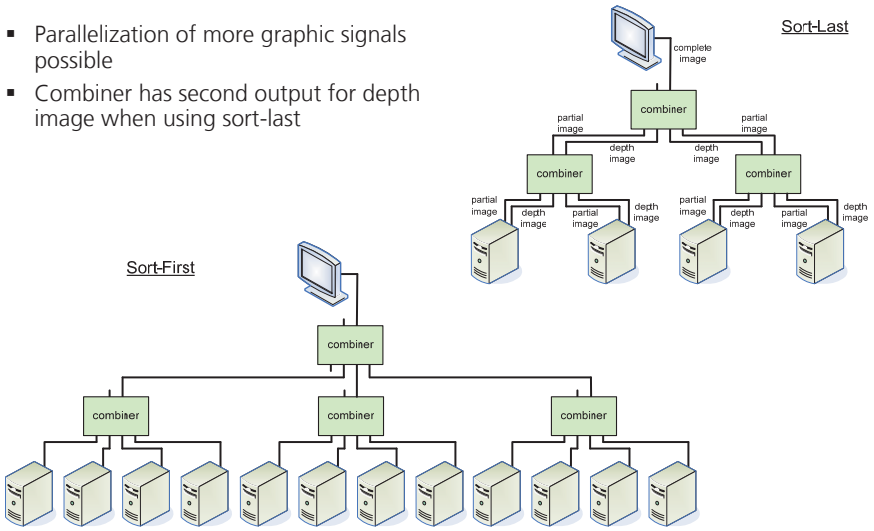
Tasks and Specification

- Input for 4 graphics signals
  - 4 partial images or
  - 2 partial images with depth information
  - ➔ 4 DVI inputs
- Output of combined image
  - Optional output of depth information for cascading
  - ➔ 2 DVI outputs
- Programmable logic for flexible combining of partial images
  - ➔ FPGA



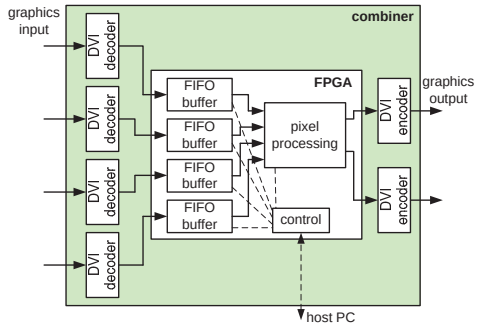
Cascading of Image Combiner

- Parallelization of more graphic signals possible
- Combiner has second output for depth image when using sort-last



Circuit Structure of Combiner

- Graphics format is DVI
  - DVI decoder and encoder for graphics signals
- Partial input images are genlocked
- Combiner has to synchronize small variations in graphics timing
  - Timing variation for hardware- and software-genlock to be determined
  - Expectation of +/- 2 lines
  - ➔ FIFO buffer using FPGA memory
- Pixel processing
- Communication with host PC



FIFO Memory

- Estimation of memory requirements with assumptions
  - Timing variation of +/- 2 lines
  - SXGA graphics format (1280 x 1024 pixel)

Required memory capacity

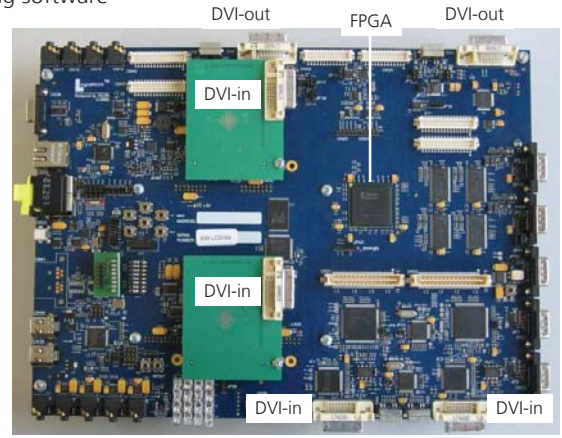
- One graphic signal is chosen as reference
- Other signals can be two lines earlier or two lines later
  - First input: FIFO of 2 lines
  - Three inputs: FIFO of 4 lines for delay of 0 to 4 lines
  - ➔ 14 lines, 1280 pixel, 24 bit per pixel require **420 kBit**

Available memory capacity

- Xilinx: Spartan-6 XC6SLX9 (second smallest) has **576 kBit** Block-RAM
- Altera: Cyclone-IV EP4CE15 (third smallest) has **504 kBit** Embedded Memory
  - ➔ Current low-cost FPGAs have sufficient internal memory

Prototype Implementation

- Prototype of combiner for system verification
  - Measurement and optimization of genlock timing
  - Development of rendering software
- Based on commercial evaluation system Xylon LogiCRAFT2
  - 2 DVI-inputs
  - 2 DVI-outputs
  - Expansion port for 2 DVI-inputs
  - Xilinx Spartan-3 1500 FPGA (576 kBit Block-RAM)



Status, Further Planning

- Evaluation hardware is running
- Current activities:
  - Set-up of synchronized parallel rendering
  - FPGA-design of prototype
  - Verification of system concept
- Next steps
  - Design of low-cost combiner board
  - Evaluation of rendering strategies and load-balancing
- Possible future activities
  - Further pixel processing, e.g. anti-aliasing

Acknowledgment

- This project is supported by the BMBF (contract number 1739X09)